

NEW UTILITY PATENT APPLICATION TRANSMITTAL

Docket No.

M4065.073/P073

JC605
U.S. PTO

(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1. 53(b))

Total Pages in this Submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Box Patent Application

Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111 (a) and 37 C.F.R. 1.53(b) is a new utility patent application for invention entitled:

METHOD OF REDUCING SURFACE CONTAMINATION IN SEMICONDUCTOR WET-PROCESSING VESSELS

and invented by:

Donald L. Yates

If a **CONTINUATION APPLICATION**, check appropriate box and supply the requisite information: Continuation Divisional Continuation-in-part (CIP) of prior application No. _____

Enclosed are:

Application Elements

- Filing fee as calculated and transmitted as described below
- Specification having 31 pages and including the following:
 - Descriptive Title of the Invention
 - Cross References to Related Applications (*if applicable*)
 - Statement Regarding Federally-sponsored Research/Development (*if applicable*)
 - Reference to Microfiche Appendix (*if applicable*)
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (*if drawings filed*)
 - Detailed Description
 - Claim(s) as Classified Below
 - Abstract of the Disclosure
- Drawing(s) (*when necessary as prescribed by 35 USC 113*)
 - Formal
 - Informal

Number of Sheets 9

NEW UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1. 53(b))

Docket No.
M4065.073/P073

Total Pages in this Submission

Application Elements (Continued)

4. Oath or Declaration

a. Newly executed (*original or copy*) Unexecuted

b. Copy from a prior application (37 CFR 1.63(d)) (*for continuation/divisional application only*)

c. With Power of Attorney Without Power of Attorney

5. Incorporation By Reference (*usable if Box 4b is checked*)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. Computer Program in Microfiche

7. Genetic Sequence Submission (*if applicable, all must be included*)

a. Paper Copy

b. Computer Readable Copy

c. Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. Assignment Papers (*cover sheet & documents*)

9. 37 CFR 3.73(b) Statement (*when there is an assignee*)

10. English Translation Document (*if applicable*)

11. Information Disclosure Statement/PTO- 1449 Copies of IDS Citations

12. Preliminary Amendment

13. Acknowledgment Postcard

14. Certificate of Mailing
 First Class Express Mail (*Specify Label No.*): _____

15. Certified Copy of Priority Document(s) (*if foreign priority is claimed*)

**NEW UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)**

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
M4065.073/P073

Total Pages in this Submission

Accompanying Application Parts (Continued)

16. Additional Enclosures (please identify below):

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	47	=	27	x \$22.00	\$594.00
Indep. Claims	8	=	5	x \$82.00	\$410.00
Multiple Dependent Claims (check if applicable)	<input type="checkbox"/>				
					0
					BASIC FEE \$790.00
OTHER FEE (specify purpose)	Assignment Recordation				
					TOTAL FILING FEE \$40.00
					\$1834.00

A check in the amount of \$1834.00 to cover the filing fee is enclosed.

The Commissioner is hereby authorized to charge and credit Deposit Account No. 04-1073, as described below. A duplicate copy of this sheet is enclosed.

Charge the amount of _____ as filing fee.

Credit any overpayment.

Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.

Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311 (b).

July 28, 1998

Dated: DICKSTEIN SHAPIRO
MORIN & OSHINSKY LLP
2101 L Street
Washington, D.C.
20037-1526



Signature
Thomas J. D'Amico

28,371

Attorney Docket No.: M4065.073/P073
Micron Docket No.: 97-1319.00/US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
APPLICATION FOR U.S. LETTERS PATENT

Title:

METHOD OF REDUCING SURFACE CONTAMINATION IN
SEMICONDUCTOR WET-PROCESSING VESSELS

Inventor:

Donald L. Yates

8682400 PCT/US2007/000000
Dickstein Shapiro Morin & Oshinsky LLP
Suite 400
2101 L Street, N.W.
Washington, D.C. 20037
(202) 785-9700

Field of the Invention

The invention relates generally to a method for reducing the
contaminants in a wet etching bath and more particularly to a method for rapidly
5 removing a substantial portion of the etching liquid from the bath such that any
contaminants are removed from the air/liquid interface of the bath surface.

10

Background of the Invention

In the fabrication of semiconductor wafers several process steps require
contacting the wafers with fluids. Examples of such process steps include etching,
15 photoresist stripping, and prediffusion cleaning. The chemicals utilized in these
steps often comprises strong acids, alkalis, or solvents. The equipment
photolithography
conventionally used for contacting semiconductor wafers with process fluid consists
of a series of tanks or sinks into which boats of semiconductor wafers are dipped.
20

Removing the wafers from the tank often results in contamination,
which is detrimental to the microscopic circuits which the fabrication process
25 creates. Since the chemicals generally are manufactured by chemical companies and
shipped to the semiconductor manufacturing plant, the initial chemical purity is
limited by the quality of the water used by the chemical manufacturers, the
container used for shipping and storing the chemical and the handling of the

chemical. Additionally, the etching bath is contaminated from the build-up of impurities both dissolved and undissolved in the process bath during the processing of the semiconductor wafers. Moreover, as chemicals age, they can become 5 contaminated with impurities from the air and from the wafers.

Thus, the etching solution must be changed periodically. The treatment of the last batch of wafers prior to fluid rejuvenation may not be as effective as 10 treatment of the first batch of wafers in a new solution. Non-uniform treatment is a major concern in semiconductor manufacturing.

In semiconductor processing involving wet etching and cleaning, bath 15 contamination at the air/liquid interface of the bath surface cannot be completely removed by air or liquid filtration. Therefore, when semiconductor wafers are removed from a wet etching/cleaning bath, the wafers become contaminated by 20 the contaminants present at the air/liquid interface of the bath.

The present invention overcomes the drawbacks of the prior etching/cleaning methods by reducing the surface contaminants in a wet etching 25 bath. The present invention provides a method for rapidly removing a substantial portion of the etching liquid from the bath such that the contaminants are removed from the air/liquid interface of the bath.

Summary of the Invention

The present invention provides a method for rapidly removing a substantial portion of the etching liquid from the bath such that the contaminants
5 are removed from the air/liquid interface of the bath surface before the wafers are removed from the bath. Rapid removal of a substantial portion of the etching liquid from the bath, reduces the amount of contaminants that are trapped by eddy currents and liquid/air surface tension forces at the surface of the bath. By rapidly removing these contaminants from the surface of the bath, the semiconductor
10 wafers can be removed from the etching bath with reduced levels of contamination on the surfaces of the wafers.

15 The above and other advantages and features of the invention will be more clearly understood from the following detailed description which is provided in connection with the accompanying drawings.

Brief Description of the Drawings

25 Fig. 1 is a perspective view of an etching bath apparatus of a first embodiment of the present invention.

Fig. 2 is a perspective view of an etching bath apparatus of a first embodiment of the present invention showing the rapid removal of the etching solution.

5

Fig. 3 is a cross-sectional view of an etching bath apparatus of a first embodiment of the present invention shown in Fig. 1.

10

Fig. 4 is a cross-sectional view of an etching bath apparatus of a first embodiment of the present invention showing the rapid removal of the etching solution as shown in Fig. 2.

15

Fig. 5 is a perspective view of an etching bath apparatus of a second embodiment of the present invention.

20

Fig. 6 is a perspective view of an etching bath apparatus of a second embodiment of the present invention showing the rapid removal of the etching solution.

25

Fig. 7 is a cross-sectional view of an etching bath apparatus of a second embodiment of the present invention shown in Fig. 5.

Fig. 8 is a cross-sectional view of an etching bath apparatus of a second embodiment of the present invention showing the rapid removal of the etching solution as shown in Fig. 6.

Fig. 9 is a perspective view of an etching bath apparatus of a third embodiment of the present invention.

5 Fig. 10 is a perspective view of an etching bath apparatus of a third embodiment of the present invention showing the rapid removal of the etching solution.

10 Fig. 11 is a perspective view of an etching bath apparatus of a fourth embodiment of the present invention.

15 Fig. 12 is a perspective view of an etching bath apparatus of a fourth embodiment of the present invention showing the rapid removal of the etching solution.

20 Fig. 13 is a side view of the baffle apparatus of a fourth embodiment of the present invention in an open flow position.

Fig. 14 is a side view of the baffle apparatus of a fourth embodiment of the present invention in a closed flow position.

25 Fig. 15 is a perspective view of an etching bath apparatus of a fifth embodiment of the present invention showing the rapid removal of the etching solution.

Fig. 16 is a microscopic photograph of a wafer processed according to a method of the present invention.

5 Fig. 17 is a microscopic photograph of a wafer processed according to a conventional method.

10 **Detailed Description of the Preferred Embodiments**

15 In semiconductor processing, various aqueous and nonaqueous solutions are employed for etching and cleaning semiconductor wafers. In many instances, much of the contamination seen in post process inspections has adsorbed to the semiconductor wafer surface while the wafer was being extracted from the wet process vessel.

20 For example, in the instance of HF chemistries, hydrophobic contamination becomes trapped at the bath surface, gathering in eddy currents. These contaminants then deposit on the hydrophobic surfaces of the wafers as they are extracted through the air/liquid interface of the processing bath.

25 Crescent shaped defect patterns are commonly seen at the edge of wafers inspected after wet cleans and are a typical indication of surface contamination. Contamination suspended in the process bath will typically take on a more random

distribution than solution or air borne contamination. However, these surface contaminants may be removed if a sufficient volume of the process solution can be rapidly removed from the top of the process vessel before a wafer is removed from the process bath. By rapidly removing a sufficient volume of the process solution, it is possible to overcome the surface tension and eddy currents between the surface contaminants at the air/liquid mixture of the etching bath and thus remove a large percentage of the surface contaminants present in the etching bath. The term "rapidly removing" used herein refers to removing a portion of the fluid from the process vessel at a flow rate sufficient to remove at least a portion of the surface contaminants on the processing fluid from the process vessel.

Exemplary processes and apparatuses for removing the surface contamination from the air/liquid interface of an etching/cleaning bath according to the present invention are described below. It is to be understood, however, that these processes and apparatuses are a few examples of many possible processes. The invention is not intended to be limited by the particular process described below.

Referring now to Fig. 1, an etching bath apparatus 10 is shown which includes an etching solution 14. It should be understood that any type of etching solution may be used in accordance with the present invention depending upon the particular substrate or material to be etched from the substrate. Examples of typical etchant solutions are those such as hydrofluoric acid solutions, potassium hydroxide

solutions or the like. It should also be understood that a cleaning solution may also be used in accordance with the present invention and that any particular cleaning bath solution may be used depending upon the materials to be cleaned.

5

The wafers 12 may be added to the etching bath apparatus 10 in order to etch the wafers 12. It should be understood that the one or a plurality of wafers may be used in accordance with the present invention in any type of mechanism, for example, a wafer boat. The wafers 12 remain in the etching solution 14 for a period of time sufficient to effectively etch the wafers 12. During the predetermined period of time that the wafers 12 remain in the etching solution 14, the etching solution 14 is fed to the etching bath apparatus and cascades over the edge 26 of the outer walls 20 of the etching bath apparatus 10 as indicated by the arrows. The etching solution 14 flows down the outer walls 20 and into the outer weir 18, where it is collected. The etching solution 14 may then be purified or cleaned and is then recycled to the etching bath apparatus 10 (not shown).

10
15
20

According to a first embodiment of the present invention, at least one outer wall 20 contains at least one upper wall component 22 (one being shown in the figure). The upper wall component 22 is hingedly connected to a lower wall component 28 of the etching bath apparatus 10 by a hinge 24. The upper wall component 22 may be latched to the adjacent outer walls 20 of the etching bath apparatus 10, as shown in Fig. 1.

It should be understood that any type of component that rapidly removes the etching solution from the etching bath apparatus 10 may work with the present invention. It should also be understood that the rapid removal of the upper portion of the etching solution may be removed from any type of etching apparatus. For example, while the figures show a cascade etching apparatus, the present invention may also be used with a static etching bath. Further, the upper portion of the etching solution may be removed from the etching apparatus during the continuous operation of a cascade flow etching bath, when the etching solution flow to a cascade flow etching bath has been stopped or in a static etching bath. For example, although the figures depict the upper wall component as a square hinged member in a cascade etching bath, it is understood that a round or other shaped hole that can be unplugged to rapidly remove the upper portion of the etching solution from the bath apparatus is also a part of the present invention. Further, it should be understood that in a preferred implementation, the portion of the etching solution that is removed is an amount sufficient to remove surface contaminants from the etching bath but not so much that the wafers in the etching apparatus are exposed.

Reference is now made to Fig. 2. After the wafers 12 have been contacted by the etching solution 14 for a sufficient period of time, the upper wall component 22 is released and the upper wall component 22 pivotally rotates about the hinge 24. Once the upper wall component 22 is released, the etching solution

14 rapidly flows from the etching bath apparatus 10 and into the outer weir 18 as indicated by the arrows.

5 Reference is now made to Figs. 3 and 4. Fig. 3 is a cross-sectional view of the etching bath apparatus 10 shown in Fig. 1. As can be seen from this figure, the wafers 12 are submerged in the etching solution 14. As the wafers are etched, surface contaminants 16 form at the air/liquid interface of the etching bath
10 apparatus 10. The contaminants 16 may be any contaminants that are formed as a result of the etching process, such as, for example silicates, polymeric silicates or the like formed from the reaction between the etching solution 14 and the wafers 12. The contaminants may also be formed from impurities in the etching chemicals.
15

As can be seen from Fig. 4, once the upper wall component 22 is released, the upper portion of the etching solution rapidly flows out of the etching bath apparatus 10. Since the flow rate of the etching solution 14 is significant, due
20 to the sudden release of the upper wall component 22, the surface tension and eddy current forces holding the contaminants 16 at the air/liquid interface are cleaved and the contaminants 16 flow into the outer weir 18 where they may be collected.
25

When the etching solution is rapidly released, the level of the etching solution 14 should be maintained such that the wafers 12 remain immersed in the

etching solution 14. The wafers 12 are then removed from the etching bath apparatus 10. Since the surface contaminants 16 have been removed from the air/liquid interface, the wafers 12 have significantly less contaminants present than if the surface contaminants 16 had not been removed.

Reference is now made to Fig. 5. This figure shows a second embodiment of the present invention. An etching bath apparatus 110 is shown which includes an etching solution 114. Wafers 112 are added to the etching bath apparatus 110 to etch the wafers 112 in a semiconductor or other process. The wafers 112 remain in the etching solution 114 for a period of time sufficient to effectively etch the wafers 112. During the predetermined period of time that the wafers 112 remain in the etching solution 114, the etching solution 114 may be added to the etching bath apparatus 110 with the overflow etching solution cascading over the edges 126 of the upper wall components 122 of the etching bath apparatus 110 as indicated by the arrows. The etching solution 114 flows down the upper wall components 122 and the lower wall components 120 and into the outer weir 118, where it may be collected.

According to a second embodiment of the present invention, the etching bath apparatus 110 contains an upper wall component 122 and the lower wall component 120. The upper wall component 122 has a slightly greater diameter than the lower wall component 120, as shown in Figs. 7 and 8. The upper wall

component 122 is held above the lower wall component 120 by any conventional apparatus and a seal is formed between the upper wall component 122 and the lower wall component 120 so that the etching solution 114 remains in the etching bath apparatus 110.

While the upper wall component 122 and the lower wall component 120 are shown in the figure as having a square cross section, it should be understood that the apparatus may take any shape, for example, the components can be circular, octagonal, rectangular or the like.

After the wafers 112 have been contacted by the etching solution 114 for a sufficient period of time, the upper wall component 122 is released and the upper wall component 122 quickly slides telescopically down the lower wall component 120 as shown in Figs. 6 and 8.

Fig. 7 is a cross-sectional view of the etching bath apparatus 110 as shown in Fig. 5. As can be seen from this figure, the wafers 112 are submerged in the etching solution 114. As the wafers are etched, surface contaminants 116 form at the air/liquid interface of the etching bath apparatus 110. As can be seen from Fig. 8, once the upper wall component 122 is released, the etching solution 114 rapidly flows out of the etching bath apparatus 110. Since the flow rate of the etching solution 114 is significant due to the sudden release of the upper wall

component 22, the surface tension and eddy current forces holding the contaminants 116 at the air/liquid interface are broken and the contaminants 116 flow into the outer weir 118 where they may be collected.

5

When the etching solution is rapidly released, the level of the etching solution 114 should be maintained such that the wafers 112 remain immersed in the etching solution 114. The wafers 112 are then removed from the etching bath apparatus 110.

10

Referring now to Fig. 9, an etching bath apparatus 210 is shown which includes an etching solution 214. Wafers 212 may be added to the etching bath apparatus 210 for etching. The wafers 212 remain in the etching solution 214 for a period of time sufficient to effectively etch the wafers 212. During the predetermined period of time that the wafers 212 remain in the etching solution 214, the etching solution may be continually refreshed to the etching bath apparatus 210 with the excess etching solution slowly cascading over the edge 226 of the outer walls 215 of the etching bath apparatus 210 as indicated by the arrows. The etching solution 214 flows down the outer wall 215 and into the outer weir 218, where it is collected.

15

20

25

According to a third embodiment of the present invention, at least one outer wall 215 contains at least one slideable door component 220 (one being

shown in the figure). The slideable door component 220 slides along the outer wall component 215 of the etching bath apparatus 210.

5 Reference is made to Fig. 10. After the wafers 212 have been contacted by the etching solution 214 for a sufficient period of time, the slideable door component 220 is released and the slideable door component 220 slides down the outer wall component 215 rapidly releasing the etching solution 214 rapidly flows 10 into the outer weir 218 as indicated by the arrows.

15 Since the flow rate of the etching solution 214 is significant due to the sudden release of the slideable door component 220, the surface tension and eddy current forces holding the contaminants at the air/liquid interface are broken and the contaminants flow into the outer weir 218. Since the surface contaminants 20 have been removed from the air/liquid interface, the wafers 212 have significantly less contaminants.

20 Referring now to Fig. 11, an etching bath apparatus 310 according to a fourth embodiment of the present invention is shown which includes etching 25 solution 315. Wafers 312 are added to the etching bath apparatus 310 in a wafer boat 314. The wafer boat 314 is fixably connected to a moveable arm 320. The moveable arm 320 is mounted on a base 335. The moveable arm 320 may move

the wafer boat 314 into or out of the etching tank 340 and may also pivot about the base 335.

5 The wafers 312 are placed in the wafer boat 314 and the wafer boat 314 is placed into the etching tank 340. The wafers 312 are immersed in the etching solution 315 for a period of time sufficient to effectively etch the wafers 312. During the predetermined period of time that the wafers 312 remain in the etching 10 solution 315, the etching solution is continuously fed from the etching solution flow throughput 325 through baffles 324 and into the etching tank 340. The flow of the etching solution 315 through the baffles 324 is indicated by arrows.

15 Reference is made to Figs. 13 and 14. The baffles 324 are open during etching to allow the etching solution 315 to flow over the wafers 312. To begin the etching process, the baffles pivot about the baffle pivots 326 from a first closed position (Fig. 14) to a second open position (Fig. 13) to allow etching solution 20 315 to flow into the etching tank 340. Once the process is completed, the baffles 324 are closed and the flow of etching solution 315 into the etching tank 340 is stopped.

25 As set forth above, the etching solution that flows through the baffles 324 flows to the top of the etching tank 340 as indicated by the arrows and cascades over the edge 313 of the outer walls 330 of the etching tank 340. The

etching solution 315 flows down the outer wall 330 and into the outer weir 318, where it is collected.

5 Reference is now made to Fig. 12. As the wafers are etched, surface contaminants form on the air/liquid interface of the etching bath tank 340. When the wafers 312 have been in contact with the etching solution 315 for a significant period of time to effectuate the necessary physical characteristics to the wafers 312, 10 the baffles 324 in the bottom of the etching tank 340 are closed. The flow of etching solution to the etching tank 340 is stopped.

15 Once the baffles 324 are closed, the wafer boat 314 is removed from the etching tank 40 and the etching solution rapidly flows out of the etching bath tank 340. After the wafers 312 have been contacted by the etching solution 315 for a sufficient period of time, the wafer boat 314 is removed from the etching tank 340 by operation of the moveable arm 320. The moveable arm 320 rapidly raises the 20 wafer boat 314 out of the etching tank 340 causing a rapid flow of the etching solution 315. Since the flow rate of the etching solution 315 is significant due to the sudden upward movement of the etching boat 314, the surface tension and 25 eddy current forces holding the contaminants at the air/liquid interface are broken and the contaminants flow into the outer weir 318 where they may be collected.

Referring now to Fig. 15, an etching bath apparatus 400 is shown which includes an etching solution 414. Wafers 412 are added to the etching bath vessel 410 for etching. According to a fifth embodiment of the present invention, after 5 the wafers 412 have been contacted by the etching solution 414 for a sufficient period of time, a paddle 420 is moved across the top of the etching bath vessel 410 rapidly displacing the etching solution 414 which then flows into the outer weir 418 together with the surface contaminants as indicated by the arrows.

10 Since the displacement of the etching solution 414 is significant because of the force of the paddle 420, the surface tension and eddy current forces holding the contaminants at the air/liquid interface are broken and the contaminants flow 15 into the outer weir 418 reducing the surface contaminants in the etching vessel.

20 Semiconductor etching apparatus may generally include from about 5 L to about 150 L of etching solution therein depending upon the particular type of applications in which the etching apparatus is used. The methods and apparatus of the present may remove from about 5% to about 75% of the etching solution from 25 the etching apparatus in order to remove accumulated surface contaminants from the etching solution. For example, in a 350mm x 350mm x 600 mm etching apparatus, about 5 to about 55 liters of the etching solution may be removed from the etching apparatus in order to remove the surface contaminants from the etching solution. In a preferred implementation, enough etching solution remains

in the etching apparatus such that the semiconductor wafers remain fully immersed in the etching solution.

5 The invention is further explained with reference to the following examples. This invention is not intended to be limited by the particular examples described below.

10 Comparative Example 1

15 Polysilicon wafers were etched in a 21.5 °C aqueous hydrofluoric acid etching solution near the end of the etching bath life. The wafers were etched for 60 seconds. The wafers were then removed from the etching bath. The wafers were examined for surface contamination defects. The wafers showed significant surface defects as can be seen in Fig. 17.

20 Example 1

25 Polysilicon wafers were etched in a 21.5 °C aqueous hydrofluoric acid etching solution near the end of the etching bath life. The wafers were etched for 60 seconds. The top of the etching bath was rapidly scraped once to remove the surface contaminants. The wafers were then removed from the etching bath. The wafers were examined for surface contamination defects. The wafers showed

significantly less surface defects than the wafers processed according to the comparative as can be seen in Fig. 16.

5 It should again be noted that although the invention has been described with specific reference to the semiconductor etching and cleaning, the invention has broader applicability and may be used in any operation where the removal of 10 contaminants from the air/liquid interface is desired. For example, the surface contamination may be removed from the surface of the etching bath by a scraping method prior to removal of the wafers from the bath. Similarly, the processes 15 described above are only several methods of many that could be used. Accordingly, the above description and accompanying drawings are only illustrative of preferred embodiments which can achieve and provide the objects, features and advantages 20 of the present invention. It is not intended that the invention be limited to the embodiments shown and described in detail herein. The invention is only limited by the spirit and scope of the following claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method for removing contaminants from a processing bath for
processing semiconductor wafers, said method comprising:

5 rapidly removing an upper portion of the semiconductor processing fluid
present in said bath while said wafers are in said bath.

10 2. The method for removing contaminants from a processing bath for
processing semiconductor wafers according to claim 1, wherein said semiconductor
processing bath is an etching bath.

15 3. The method for removing contaminants from a processing bath for
processing semiconductor wafers according to claim 1, wherein said semiconductor
processing bath is a cleaning bath.

20 4. The method for removing contaminants from a processing bath for
processing semiconductor wafers according to claim 1, wherein said contaminants
are removed from the air/liquid interface of the semiconductor processing bath.

25 5. The method for removing contaminants from a processing bath for
processing semiconductor wafers according to claim 4, wherein said wherein said
semiconductor processing bath is an etching bath.

6. The method for removing contaminants from a processing bath for processing semiconductor wafers according to claim 5, wherein said wherein said contaminants include silica.

5

7. A method for reducing the contamination on a semiconductor wafer from a wet etching bath comprising:

10 processing said semiconductor wafer in said wet etching bath;

15 subsequently rapidly removing an upper portion of the etching fluid from said wet etching bath to remove contaminants from the surface of said wet etching bath while retaining said semiconductor wafer in said etching bath; and,

20 subsequently removing said semiconductor wafer from said wet etching bath.

25 8. The method for reducing the contamination on a semiconductor wafer from a wet etching bath according to claim 7, wherein a substantial portion of said etching fluid is removed.

9. The method for reducing the contamination on a semiconductor wafer from a wet etching bath according to claim 8, wherein said upper portion of said etching fluid is removed by draining a top portion of said etching fluid from said wet etching bath.

10. The method for reducing the contamination on a semiconductor wafer from a wet etching bath according to claim 9, wherein said upper portion of said etching fluid is removed by a paddle from the top of said wet etching bath.

5

11. The method for reducing the contamination on a semiconductor wafer from a wet etching bath according to claim 9, wherein said upper portion of said etching fluid is removed by opening a valve in said wet etching bath.

10

12. The method for reducing the contamination on a semiconductor wafer from a wet etching bath according to claim 9, wherein said upper portion of said etching fluid is removed by hingedly releasing a door located at an upper portion of said wet etching bath.

15

13. The method for reducing the contamination on a semiconductor wafer from a wet etching bath according to claim 9, wherein said upper portion of said etching fluid is removed by sliding a door located at an upper portion of said wet etching bath.

20

14. The method for reducing the contamination on a semiconductor wafer from a wet etching bath according to claim 9, wherein said upper portion of said etching fluid is removed by rapidly removing a wafer boat containing said semiconductor wafer from said wet etching bath.

15. The method for reducing the contamination on a semiconductor wafer from a wet etching bath according to claim 9, wherein said upper portion of said etching fluid is removed by telescopically collapsing said wet etching bath.

5

16. The method for reducing the contamination on a semiconductor wafer from a wet etching bath according to claim 10, wherein said contaminants are removed from the air/liquid interface of said wet etching bath.

10

17. A method for etching a semiconductor wafer, said method comprising:

15

placing etching fluid into an etching vessel;

placing said semiconductor wafer in said etching fluid;

20

contacting said semiconductor wafer with said etching fluid for a predetermined time;

25

rapidly removing a portion of said etching fluid from the upper surface of said etching vessel while keeping said semiconductor wafer immersed in said etching fluid; and,

removing said semiconductor wafer from said etching fluid.

18. The method according to claim 17, wherein said semiconductor wafer is a silicon wafer.

5 19. The method according to claim 18, wherein said etching fluid is an aqueous hydrofluoric acid solution.

10 20. The method according to claim 17, wherein said etching fluid is removed from the upper surface of said etching vessel by draining a top portion of said etching fluid from said wet etching vessel.

15 21. The method according to claim 20, wherein said upper portion of said etching fluid is removed by opening a valve in said wet etching vessel.

20 22. The method according to claim 20, wherein said upper portion of said etching fluid is removed by hingedly releasing a door located at an upper portion of said wet etching vessel.

25 23. The method according to claim 20, wherein said upper portion of said etching fluid is removed by sliding a door located at an upper portion of said wet etching vessel.

24. The method according to claim 20, wherein said upper portion of said etching fluid is removed by rapidly removing a wafer boat containing said semiconductor wafers from said wet etching vessel.

25. The method according to claim 20, wherein said upper portion of said etching fluid is removed by telescopically collapsing said wet etching vessel.

5 26. The method according to claim 17, wherein said etching fluid is removed from the upper surface of said etching vessel by physically removing a top portion of said etching fluid from said wet etching vessel.

10 27. The method according to claim 26, wherein said upper portion of said etching fluid is removed from said etching vessel by a paddle.

15 28. An etching bath apparatus for reducing the contamination of semiconductor wafers during wet processing, said apparatus comprising:

an etching vessel having a sufficient volume to hold a predetermined amount of etching fluid;

20 said etching vessel having a plurality of side walls, at least one of said plurality of side walls having at least one gate located near the top of said side walls to rapidly remove a portion of etching fluid from said etching vessel.

25 29. The etching bath apparatus according to claim 28, wherein etching fluid is continuously fed into said etching vessel during processing and the excess etching fluid is removed by cascading over the top of the plurality of side walls of said etching vessel.

30. The etching bath apparatus according to claim 29, wherein said etching vessel has a single gate to remove to rapidly remove an upper portion of etching fluid from said etching vessel.

5

31. The etching bath apparatus according to claim 30, wherein said upper portion of said etching solution is rapidly removed during the cascade operation.

10

32. The etching apparatus according to claim 30, wherein said gate is hingedly attached to one of said side walls.

15

33. The etching apparatus according to claim 30, wherein said at least one gate is slideably mounted to one of said plurality of walls.

20

34. The etching apparatus according to claim 33, wherein said apparatus has a single gate.

35. An etching vessel comprising:

a first hollow container;

25

a second hollow container;

5
said first hollow container being located beneath said second hollow container and sealingly engaged to said second hollow container such that said first and said second hollow containers form said etching vessel;

10
said first hollow container and said second hollow container having a size such that said second hollow container can slide over said first hollow container;

15
said etching vessel having a sufficient volume to hold a predetermined amount of etching fluid; and

20
25
wherein said second hollow container is moveable relative to said first hollow container to rapidly remove said etching fluid from an upper portion of said etching vessel.

36. The etching vessel according to claim 35, wherein etching fluid is continuously fed into said etching vessel and the excess etching fluid is removed by cascading over the top said second hollow container.

37. An etching bath apparatus comprising:

25
an etching vessel, said etching vessel including means for rapidly removing a portion of the etching fluid from the upper portion of said etching vessel.

38. The etching bath apparatus according to claim 37, wherein said means for rapidly removing a portion of the etching fluid from the upper portion of said etching vessel includes a gate.

5

39. The etching bath apparatus according to claim 37, wherein said means for rapidly removing a portion of the etching fluid from the upper portion of said etching vessel includes a slideable door.

10

40. The etching bath apparatus according to claim 37, wherein said means for rapidly removing a portion of the etching fluid from the upper portion of said etching vessel includes a door.

15

41. The etching bath apparatus according to claim 35, wherein said means for rapidly removing a portion of the etching fluid from the upper portion of said etching vessel includes a valve.

20

42. The etching bath apparatus according to claim 37, wherein said means for rapidly removing a portion of the etching fluid from the upper portion of said etching vessel includes a paddle.

25

43. The etching bath apparatus according to claim 37, wherein said means for rapidly removing a portion of the etching fluid from the upper portion of said etching vessel includes a collapsible member.

44. A method for reducing the contaminants on a silicon wafer during a wet etching process, said method comprising:

5 immersing a wafer boat in an etching vessel having an etching fluid therein for a sufficient time to etch said silicon wafer;

10 rapidly removing said semiconductor boat from said etching vessel to remove contaminants residing on the upper surface of said etching fluid.

15 45. An apparatus for wet processing semiconductor wafers to reduce the contamination on the silicon wafer during a wet process, said apparatus comprising:

20 an etching vessel;

a semiconductor wafer boat;

25 a system for rapidly removing said semiconductor wafer boat from said etching vessel to remove surface contaminants from the etching fluid before said semiconductor wafers are removed from said etching fluid; and

an outer weir.

46. The apparatus according to claim 45, wherein said etching vessel has baffles located at the bottom of said etching vessel to selectively allow etching fluid to flow past said wafer boat.

5

47. The apparatus according to claim 45, wherein said system includes a moveable arm which is fixably mounted to said wafer boat.

10

15

20

25

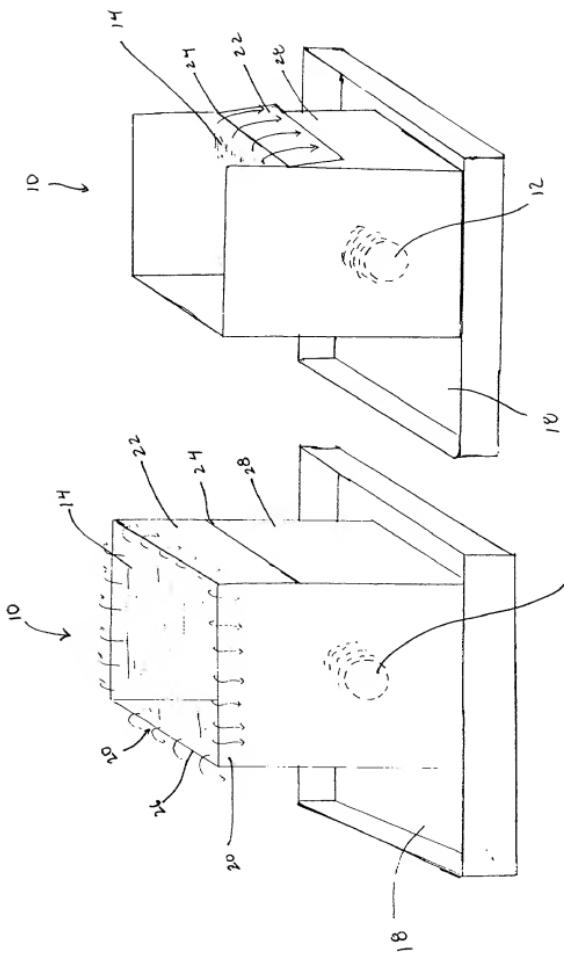
ABSTRACT

A method and apparatus for reducing the contaminants in a wet etching bath by rapidly removing a substantial portion of the etching liquid from the bath such that the contaminants are removed from the air/liquid interface of the bath surface is described. By rapidly removing a substantial portion of the etching liquid from the bath, contaminants that are trapped by eddy currents and liquid/air surface tension forces are greatly reduced at the surface of the bath. The semiconductor wafers treated showed reduced levels of contamination.

卷之三

510

25



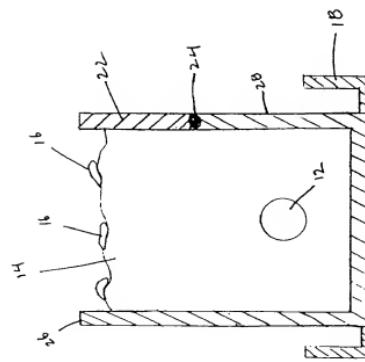


FIG. 3

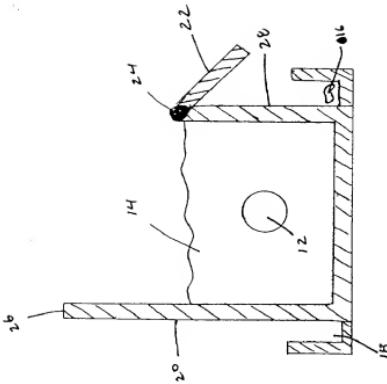


FIG. 4

FIG. 6

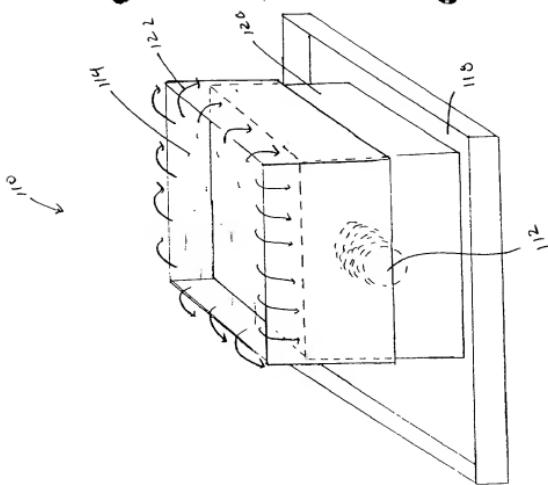
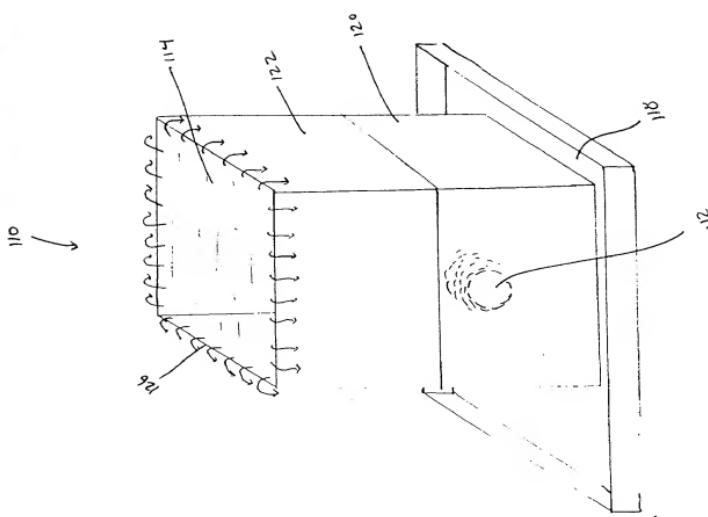


FIG. 5



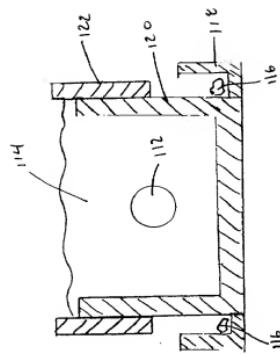


FIG. 8

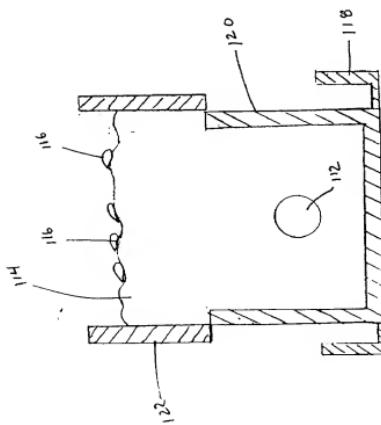


FIG. 7

FIG. 10

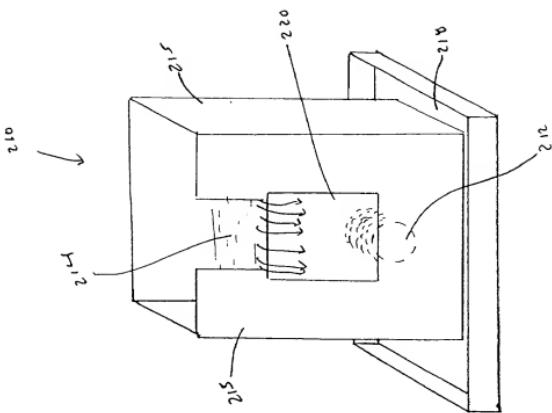
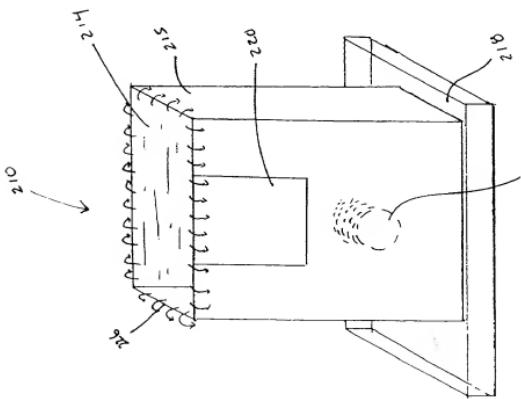


FIG. 9



320

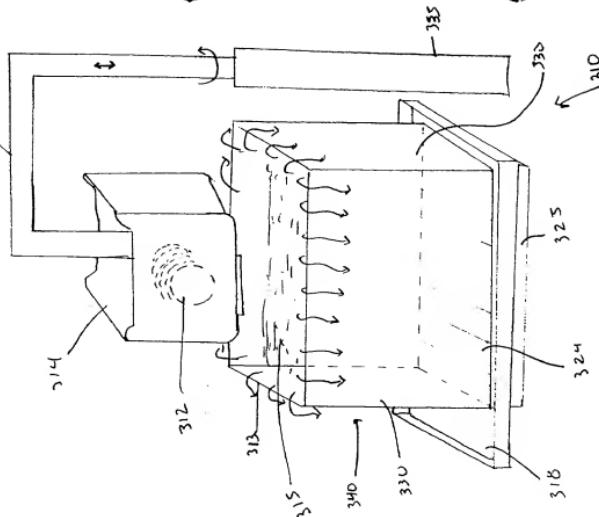


FIG. 12

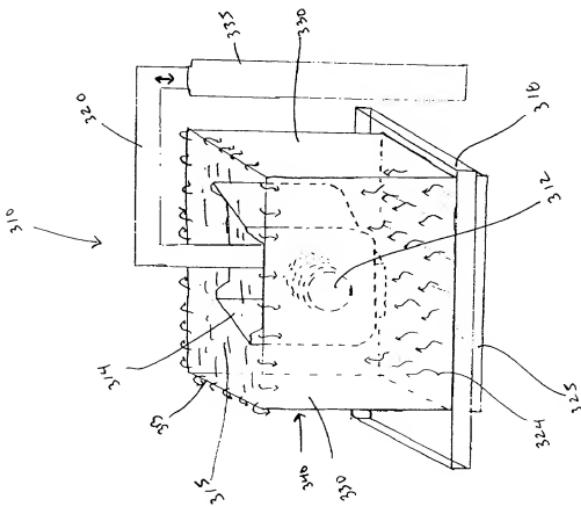


FIG. 11

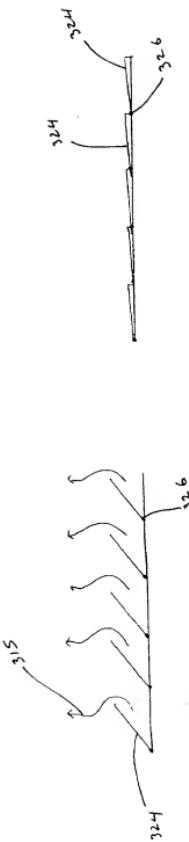


FIG. 13 14

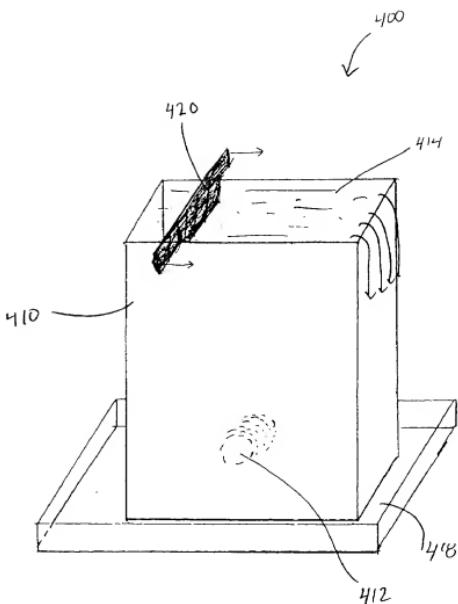


FIG. 15

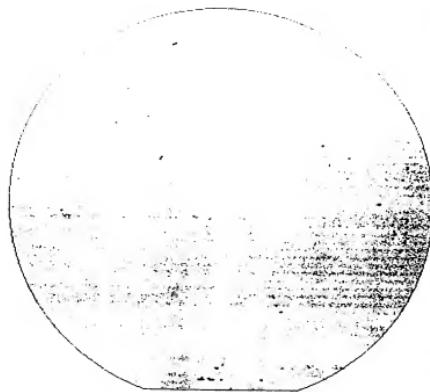


FIG. 16

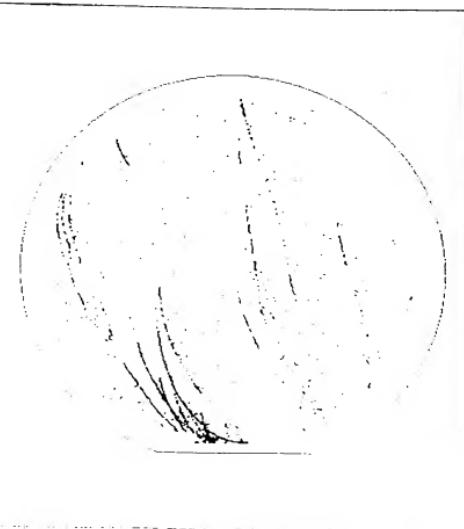


FIG. 17

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**METHOD OF REDUCING SURFACE CONTAMINATION IN
SEMICONDUCTOR WET-PROCESSING VESSELS.**

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

None

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

None

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please address all correspondence to Thomas J. D'Amico of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street, NW, Washington, DC 20037-1526. Telephone calls should be made to Thomas J. D'Amico by dialing (202) 828-2232.

Full name of 1st joint inventor: Donald L. Yates

Inventor's signature Donald L. Yates Date 7/24/98

Residence: Boise, Idaho

Citizenship: United States of America

Post Office Address: P.O. Box 16576, Boise, Idaho 83715

PATENT
Docket No.: M4065.073/P073
Micron No.: 97-1319.00/US

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Patent Application
Inventor: Donald L. YATES

Serial No.: Not Yet Assigned Group Art Unit: Not Yet Assigned

Filed: Concurrently Herewith Examiner: Not Yet Assigned

For: METHOD OF REDUCING
SURFACE
CONTAMINATION IN
SEMICONDUCTOR WET-
PROCESSING VESSELS

POWER OF ATTORNEY BY ASSIGNEE AND
CERTIFICATE BY ASSIGNEE UNDER 37 C.F.R. § 3.73(b)

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by virtue of the assignment attached hereto (which is also being submitted concurrently for recordation), hereby appoints the attorneys and agents of the firm of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street, NW, Washington, DC 20037-1526, listed as follows: Gary M. Hoffman, 26,411; Thomas J. D'Amico, 28,371; Donald A. Gregory, 28,954; James W. Brady, Jr., 32,115; Jon D. Grossman, 32,699; Mark J. Thronson, 33,082; Laurence D. Fisher,

37,131; John R. Fuisz, 37,327; Juliana Haydoutova, P43,313; James M. Heintz, P41,828; Herbert V. Kerner, P42,721; Gianni Minutoli, 41,198; Eric Oliver, 35,307; William E. Powell, III, 39,803; James M. Silbermann, 40,413; Richard Veltman, 36,957 and Darius Gambino, 41,472, and also attorneys Michael L. Lynch, 30,871; Lia M. Pappas, 34,095; W. Eric Webostad, 35,406; and Charles B. Brantley, II, 38,086 of Micron Technology, Inc. as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above-identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

Thomas J. D'Amico, Esq.
Dickstein Shapiro Morin & Oshinsky LLP
2101 L Street, NW
Washington, D.C. 20037-1526
Telephone: (202) 828-2232
Facsimile: (202) 887-0689

MICRON TECHNOLOGY, INC.


Michael L. Lynch
Chief Patent Counsel
Registration No. 30,871

Dated: 2/27/98